Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method for packet processing comprising,
   a) obtaining first information regarding a packet;
   b) using the first information as an index into a parser memory;
   c) retrieving from the parser memory an entry comprising a location in the packet of one or more protocol bits specifying a protocol associated with the packet;
   d) obtaining a match engine index; and,
   e) using the protocol bits and the match engine index as a key to retrieve a match engine entry from a match engine memory, the match engine entry comprising an action to take on the packet.

2. (Original) The method of claim 1 wherein the match engine index is included in the parser memory entry.

3. (Original) The method of claim 1 wherein the parser memory entry comprises a context memory base address and either a location in the packet of a set of label bits or an indication that there are no label bits,

   wherein, if the parser memory entry includes a location of a set of label bits, the method comprises retrieving from the packet the label bits, and obtaining the match engine index comprises using the context memory base address and label bits to retrieve from a context memory an entry comprising the match engine index.

4. (Original) The method of claim 3 wherein, if the location in the packet of a set of label bits indicates that there are no label bits, obtaining the match engine index comprises retrieving a match engine index included in the parser memory entry.

5. (Original) The method of claim 4 wherein the match engine memory comprises a content-addressable memory.

6. (Original) The method of claim 4 wherein the match engine memory comprises a ternary content-addressable memory.

7. (Original) The method of claim 1 wherein the match engine memory comprises a content-addressable memory.

8. (Original) The method of claim 1 wherein obtaining the first information comprises identifying a channel with which the packet is associated.

9. (Original) A method for packet processing in a packet processing system, the method comprising:

a step for obtaining first information regarding a packet;

a step for retrieving an entry corresponding to the first information from a parser memory;

a step for retrieving from the packet one or more protocol bits identified by the parser memory entry;

a step for retrieving from a match engine memory a match engine memory entry comprising an action to perform using a match engine key comprising a combination of the protocol bits and a match engine index; and,

a step for performing the action specified in the retrieved match engine entry.

10. (Original) The method of claim 9 wherein the action comprises extracting information relating to another protocol from the packet.

11. (Original) The method of claim 9 wherein the action is selected from the group consisting of forwarding the packet, discarding the packet, adding additional header information to the packet, associating the packet with a quality of service level, and extracting information relating to another protocol from the packet.

12. (Original) A packet processing apparatus comprising:
a control logic circuit;

a parser memory accessible to the control logic circuit the parser memory comprising a plurality of entries each specifying a location in a packet of one or more protocol bits and at least some of which specifying a match engine index;

a match engine memory accessible to the control logic circuit, the match engine memory comprising a plurality of entries each specifying an action to be taken; and,

a context memory accessible to the control logic circuit, the context memory comprising a plurality of entries each specifying a match engine index;

wherein the control logic circuit is configured to generate a match engine key by combining protocol bits of a packet identified in a parser memory entry with a match engine index from an entry of either the parser memory or the context memory, to retrieve from the match engine memory an entry corresponding to the match engine key, and to perform an action specified in the match engine entry.

13. (Original) The apparatus of claim 12 wherein the control logic circuit comprises an integrated circuit and the parser memory is integrated with the control logic circuit.

14. (Original) The apparatus of claim 12 wherein the control logic circuit comprises an integrated circuit and the match engine memory is integrated with the control logic circuit.

15. (Original) The apparatus of claim 14 wherein the control logic circuit comprises an integrated circuit and the parser memory is integrated with the control logic circuit.

16. (Original) The apparatus of claim 15 wherein the context memory is external to the control logic circuit and the control logic circuit comprises an integrated interface to the context memory.

17. (Original) The apparatus of claim 16 wherein the parser memory comprises 512 or fewer entries.

18. (Original) The apparatus of claim 17 wherein the match engine memory comprises 512 or fewer entries.

19. (Original) The apparatus of claim 16 wherein the control logic circuit comprises a pipelined architecture.

20. (Currently Amended) A configurable device for processing packets, the device supporting a plurality of protocols, the device comprising:

a first internal memory comprising a plurality of entries;

a second internal memory comprising a plurality of entries each comprising an action to be taken on the packet;

logic circuitry for identifying a channel value associated with the packet, retrieving an entry from the first memory using the channel value as an index, and obtaining from the entry address information identifying a set of entries in an external context memory applicable to the channel value;

logic circuitry for ~~using~~ combining the address information ~~and~~ with one or more bit values from the packet to create a key and to use the key to retrieve from the external context memory one entry from the set of entries; and,

logic circuitry for using information from the one entry retrieved from the external context memory to retrieve from the second memory an action to be taken on the packet.

21. (Original) The device of claim 20 wherein the action to be taken on the packet comprises extracting information relating to a protocol from the packet.

22. (Original) The device of claim 21 wherein the second memory comprises a content addressable memory.

23. (Original) The device of claim 22 wherein the first memory comprises a random access memory.

24. (Original) A packet processing device comprising:
means for retrieving first information about a received packet;
means for retrieving an entry corresponding to the first information, the entry comprising a location in the packet of one or more protocol bits specifying a protocol associated with the packet and a match engine index;
means for generating a match engine key; and,
means for retrieving an action corresponding to one of a plurality of match engine entries which matches the match engine key; and,
means for performing the action.

25. (Original) The packet processing device of claim 24 wherein the first information comprises an ATM channel associated with the packet.

26. (Original) The packet processing device of claim 25 wherein the means for performing the action included means for forwarding the packet to another packet processing device.

27. (Currently Amended) The packet processing device of claim 24 comprising means for determining from the entry whether or not to retrieve an entry from an external context memory and, means for retrieving an entry from the external context memory, wherein the means for

generating the match engine key is adapted to generate the match engine key using information in the entry from the external context memory.

28. (Original) The packet processing device of claim 27 wherein the means for generating a match engine key, the means for retrieving an action and the means for retrieving an entry from the external context memory are incorporated on a single integrated circuit.